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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,552	07/06/2005	Mitsuhiro Yamamoto	274746US2PCT	8157

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1940 DUKE STREET
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EXAMINER	
HAILEMARIAM, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
08/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/541,552	YAMAMOTO, MITSUHIRO	
	Examiner	Art Unit	
	Emmanuel Hailemariam	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :03/02/07, 11/30/06 and 10/11/05.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1- 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Ha et al. (US 20040207593).

As to claim 1, Ha discloses an array substrate (22) for a flat display device [0011] comprising: a display unit in which a pixel is placed at each of intersections between a plurality of signal lines (fig.1-DL); and a plurality of scan lines (fig.1GL), the signal and scan lines being routed in the form of a matrix; a plurality of output lines (fig.1- PD, [0012], [0016] configured to output data signals to the signal lines, respectively; a plurality of switches placed between the output lines and the signal lines to connect each output line to n signal lines (n is an integer equal to or greater than two) one after another within one horizontal period; n switch control (24) signal lines (fig.2(29)and fig.18 (69)) configured to supply control electrodes of the switches with control signals for controlling on and off states thereof, and a plurality of electrode patterns configured to connect the control electrode of each switch to any one of the n switch control

Signal lines (fig.1-DL); wherein the electrode patterns each two-dimensionally overlap all of the switch control signal lines and have substantially identical shapes [0014].

As to claim 2, Ha discloses that the electrode patterns and the switch control signal lines are stacked with an insulating layer interposed there (fig.1 and 2, and 5A-8B), and are electrically connected to each other by contact holes formed in the insulating layer [0006, the insulating layer is covering the electrical part that conducts electrical signal).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1- 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards. (20030107544 A1).

As to claim 1, Edwards discloses an array substrate for a flat display device [0021] comprising: a display unit (10) in which a pixel (12) is placed at each of intersections between a plurality of signal lines (fig.1 (1), (2)); and a plurality of scan lines (fig.1 (1), (2), the signal and scan lines being routed in the form of a matrix; a plurality of output lines configured to output data signals to the signal lines (fig.1 (1), (2), n-1, n) respectively; a plurality of switches placed between the output lines and the signal lines to connect each output line to n signal lines (n is an integer equal to or greater than two)

one after another within one horizontal period; n switch control (21) signal (fig.1(1), (2),n-1, n) configured to supply control electrodes of the switches with control signals for controlling on and off states thereof, and a plurality of electrode patterns configured to connect the control electrode of each switch to any one of the n switch control signal lines(fig.1(1), (2),n-1, n) wherein the electrode patterns each two-dimensionally overlap all of the switch control signal lines and have substantially identical shapes .

Number of signal lines (N) are not taught directly however it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a plurality of signal lines [0003], [0004]. This is common and well known in the art.

As to claim 2, Edwards discloses array substrates according to claim 1, wherein the electrode patterns and the switch control signal lines are stacked with an insulating layer interposed there between, and are electrically connected to each other by contact holes formed in the insulating layer ([0035], [0037] (fig.1 (1, 2), n-1- n).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Hailemariam whose telephone number is 571-270-1545. The examiner can normally be reached on M-F 8:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-1550. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Emmanuel Hailemariam 07/20/07

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER